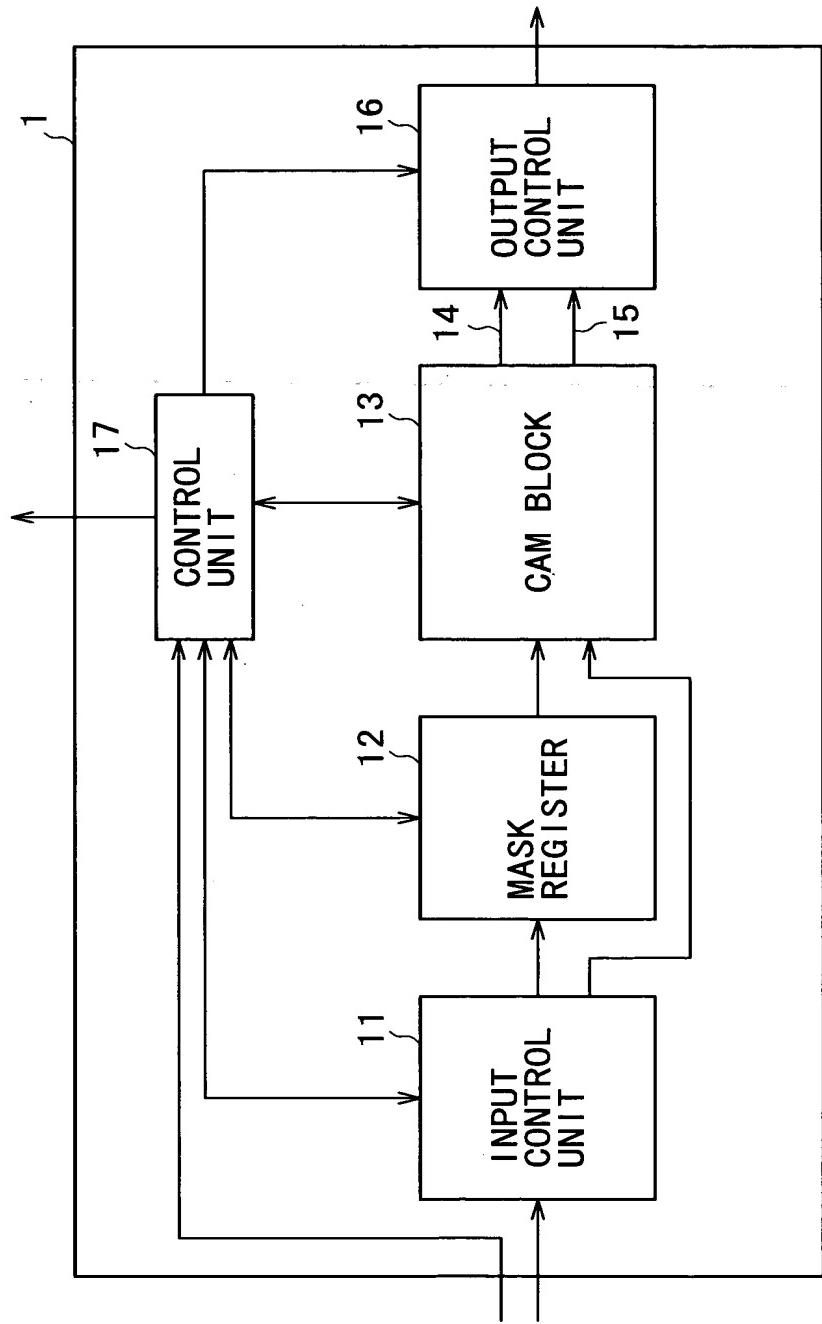


FIG. 1

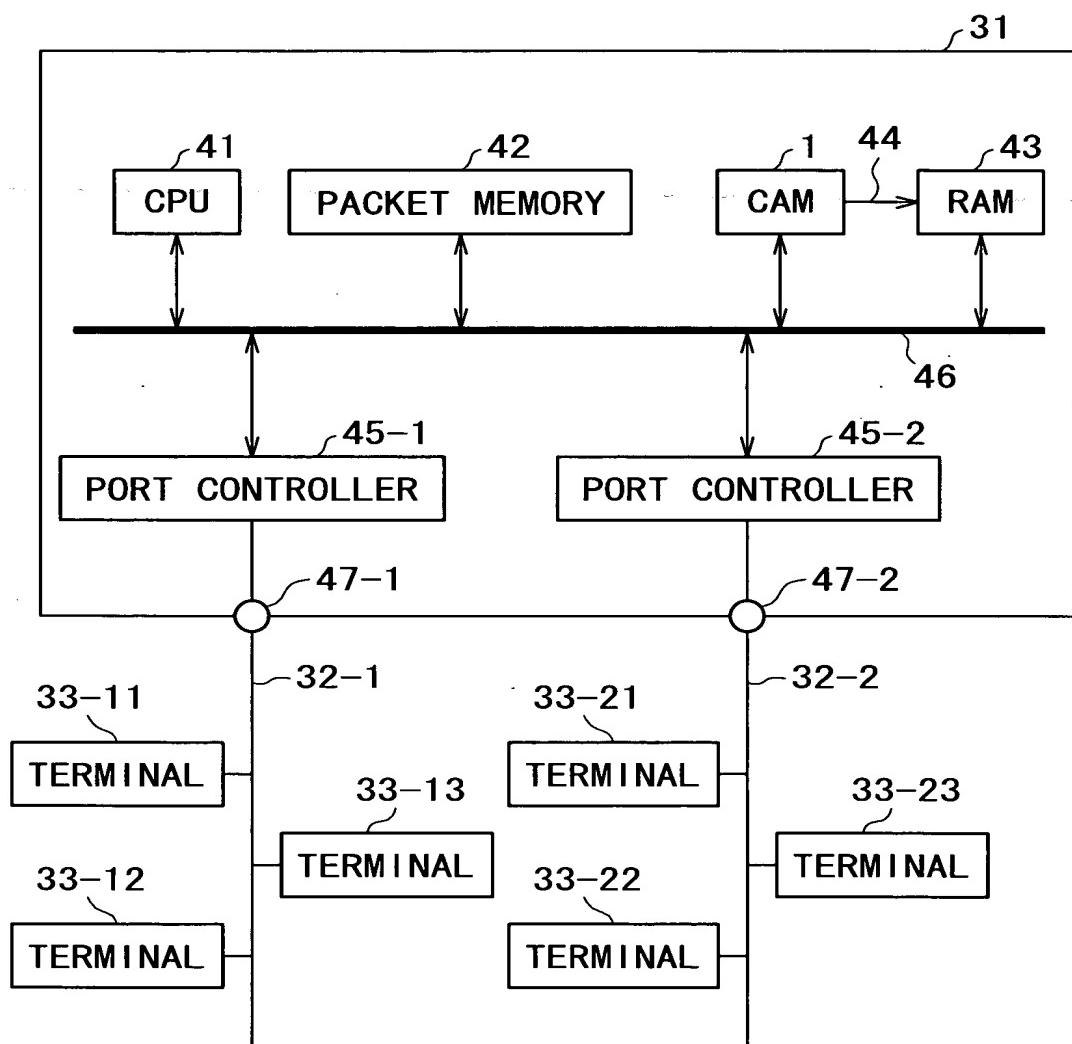


F I G. 2

The diagram illustrates a memory structure with three columns: ADDRESS, STORED DATA, and EMPTY BIT. A bracket above the first two columns is labeled 'm', indicating they together form an address of width m. The first row, labeled ~21-1, shows an address of three 'x' characters, stored data of three 'x' characters, and an empty bit of 1. The second row, labeled ~21-2, shows an address of three 'x' characters, stored data of three 'x' characters, and an empty bit of 0. Ellipses below the first row indicate additional entries.

ADDRESS	STORED DATA	EMPTY BIT
xxx	xxx	1
xxx	xxx	0
⋮	⋮	

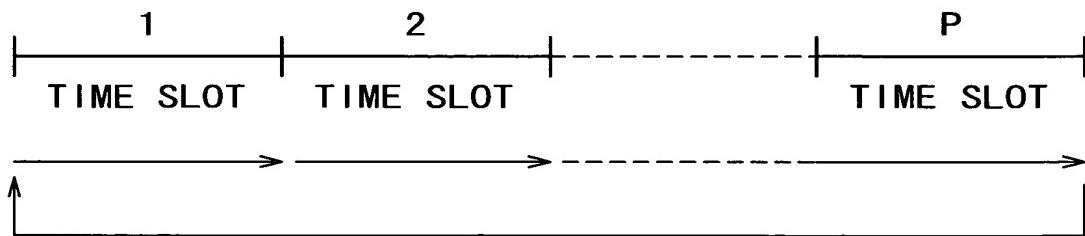
F I G. 3



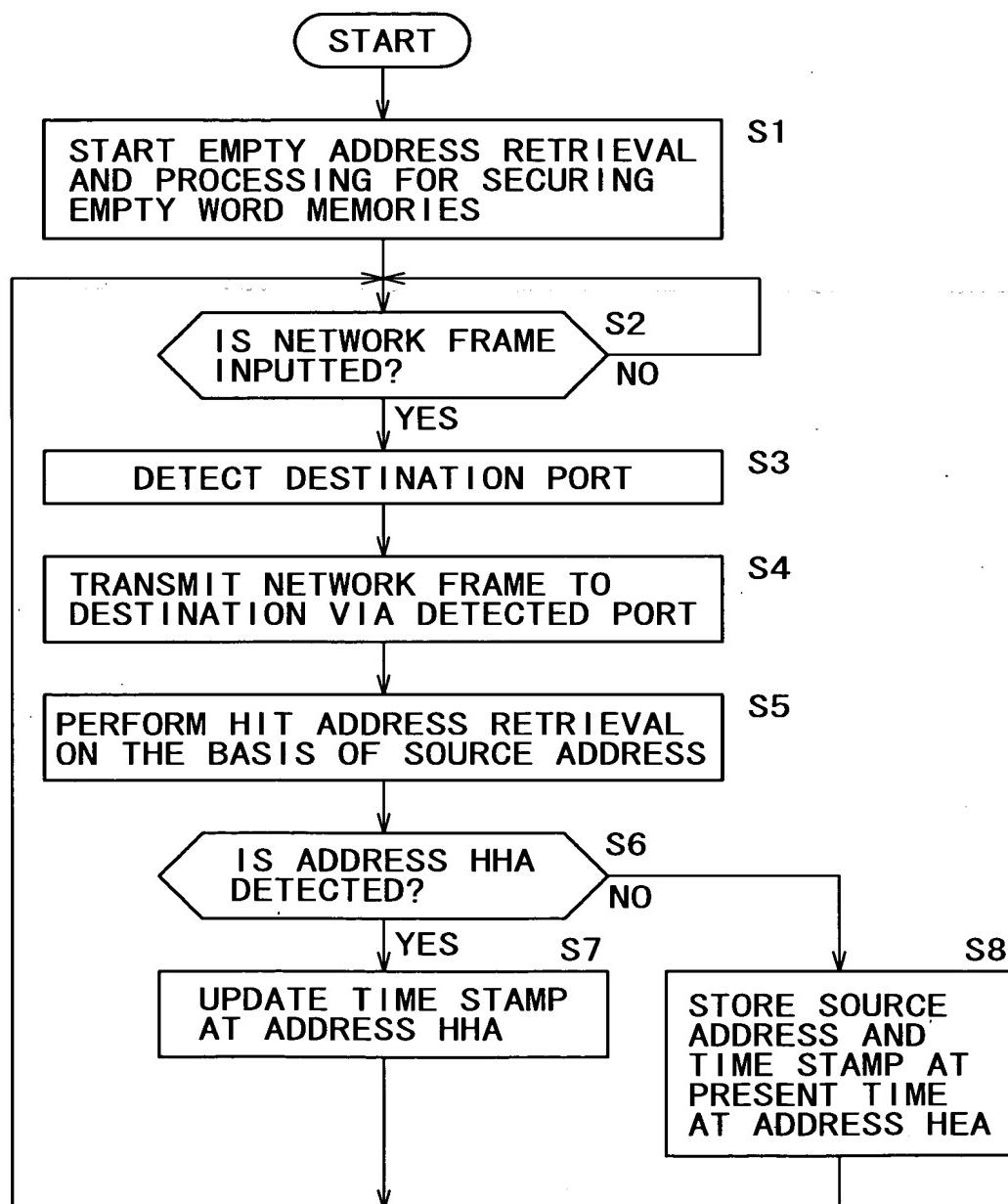
F I G. 4

ADDRESS	STORED DATA		EMPTY BIT	
xxx	NETWORK ADDRESS OF TERMINAL 33-11	TIME STAMP	1	~21-1
xxx	NETWORK ADDRESS OF TERMINAL 33-12	TIME STAMP	0	~21-2
:	:	:		

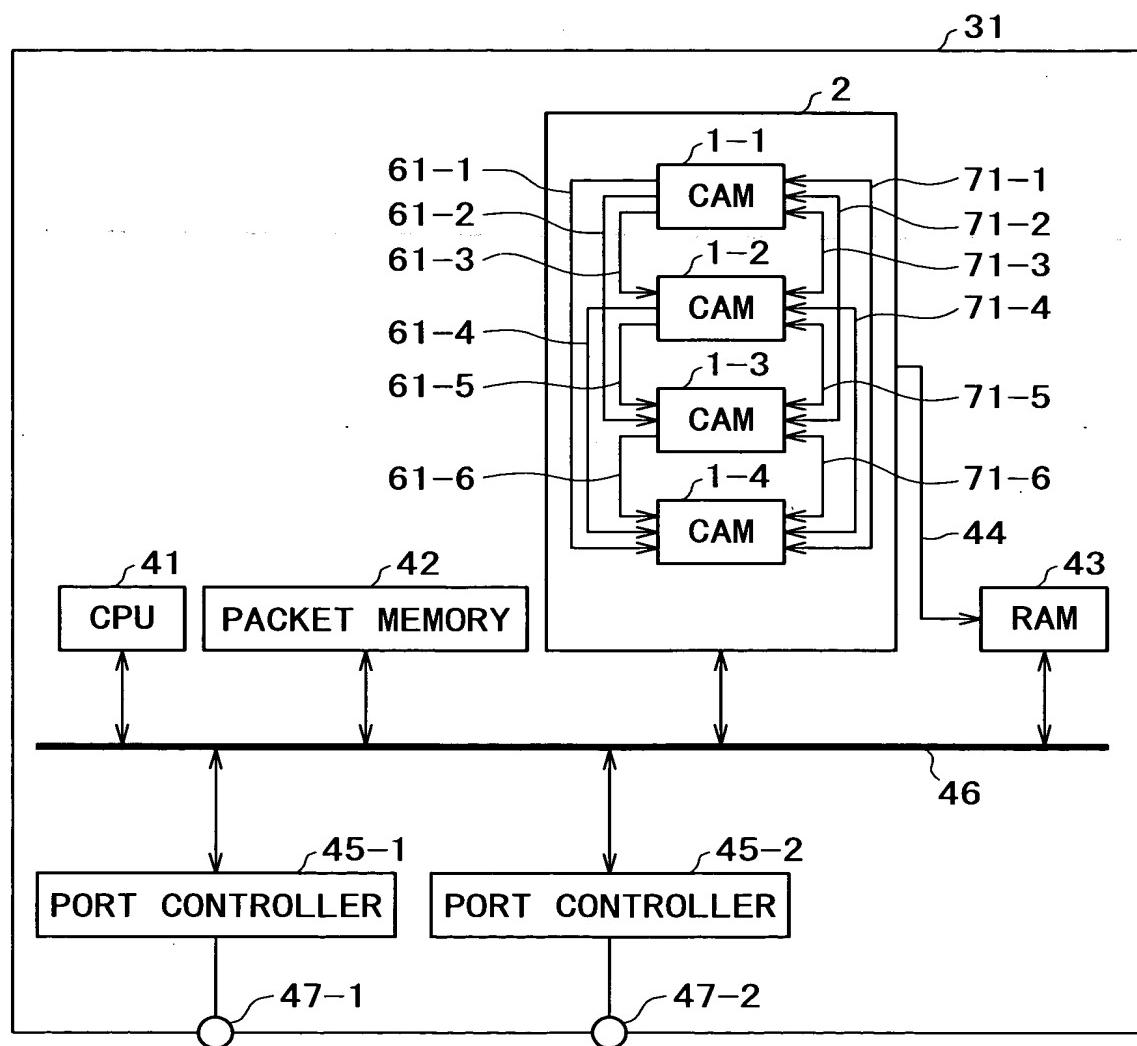
F I G. 5



F I G. 6



F I G. 7



F I G. 8

LOW

ADDRESS	STORED DATA	EMPTY ADDRESS
xxx	xxx	1
:	:	
ADDRESS	STORED DATA	EMPTY ADDRESS
xxx	xxx	0
:	:	
ADDRESS	STORED DATA	EMPTY ADDRESS
xxx	xxx	1
:	:	
ADDRESS	STORED DATA	EMPTY ADDRESS
xxx	xxx	0
:	:	

HIGH

1-1

1-2

1-3

1-4

F I G. 9

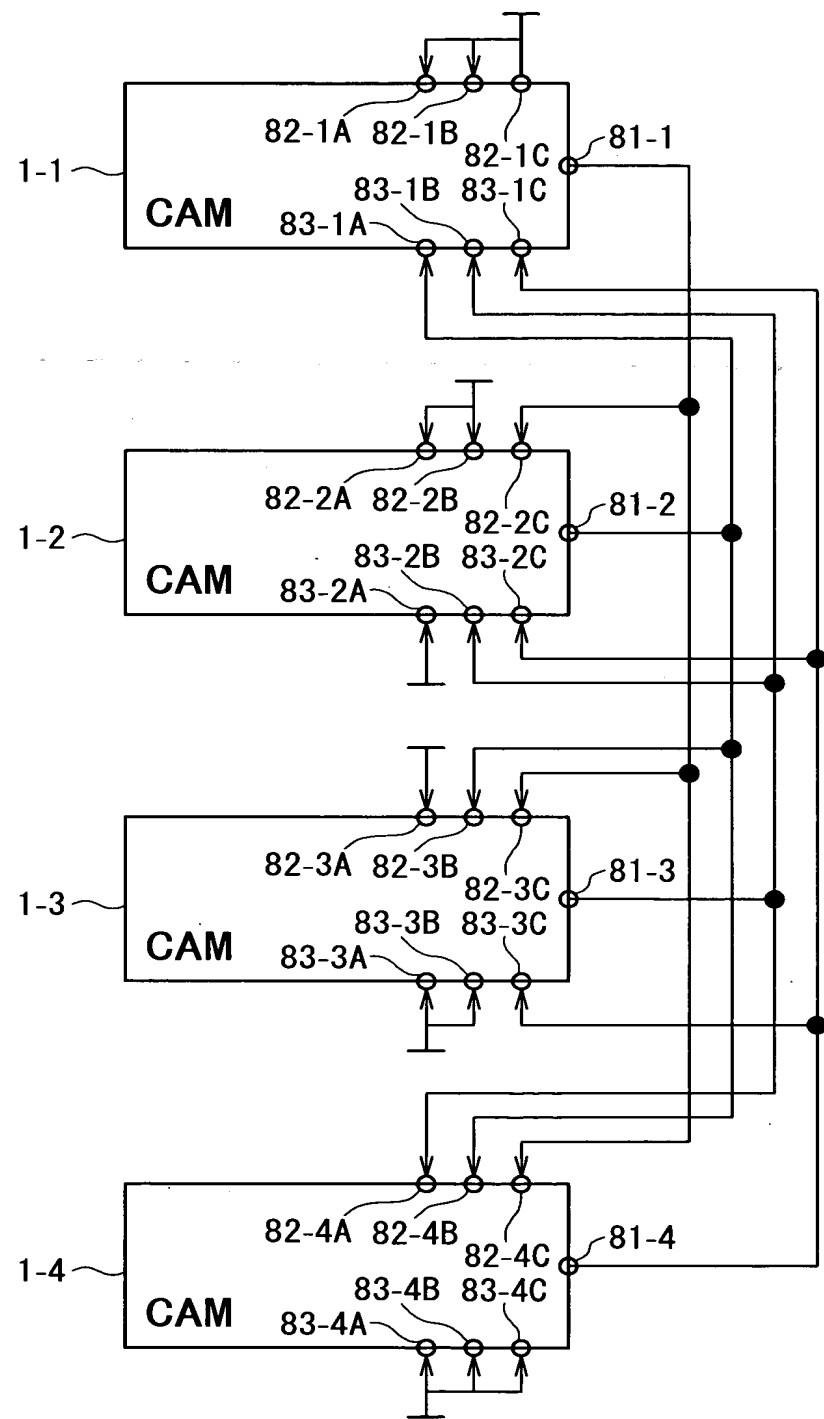
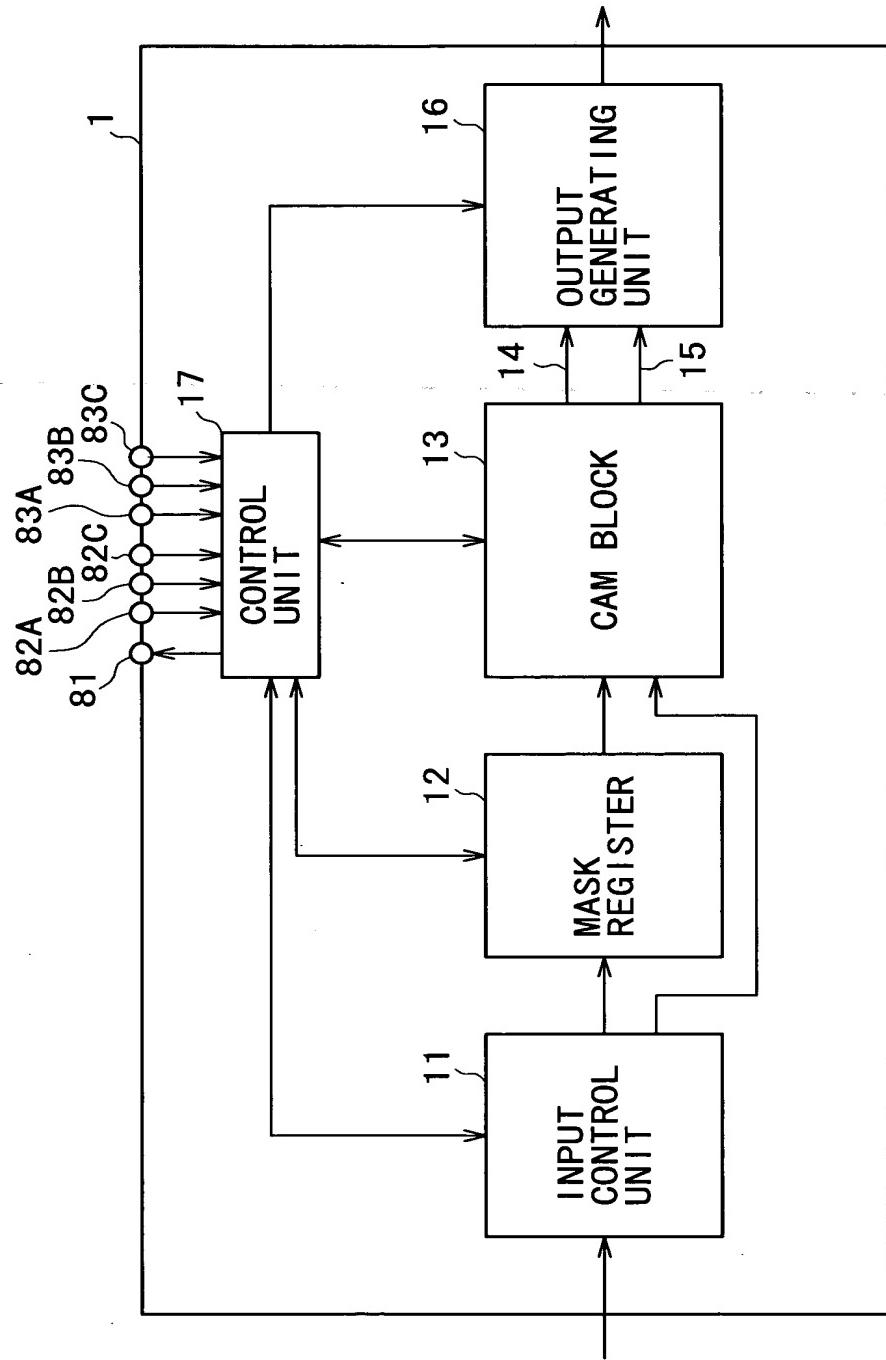
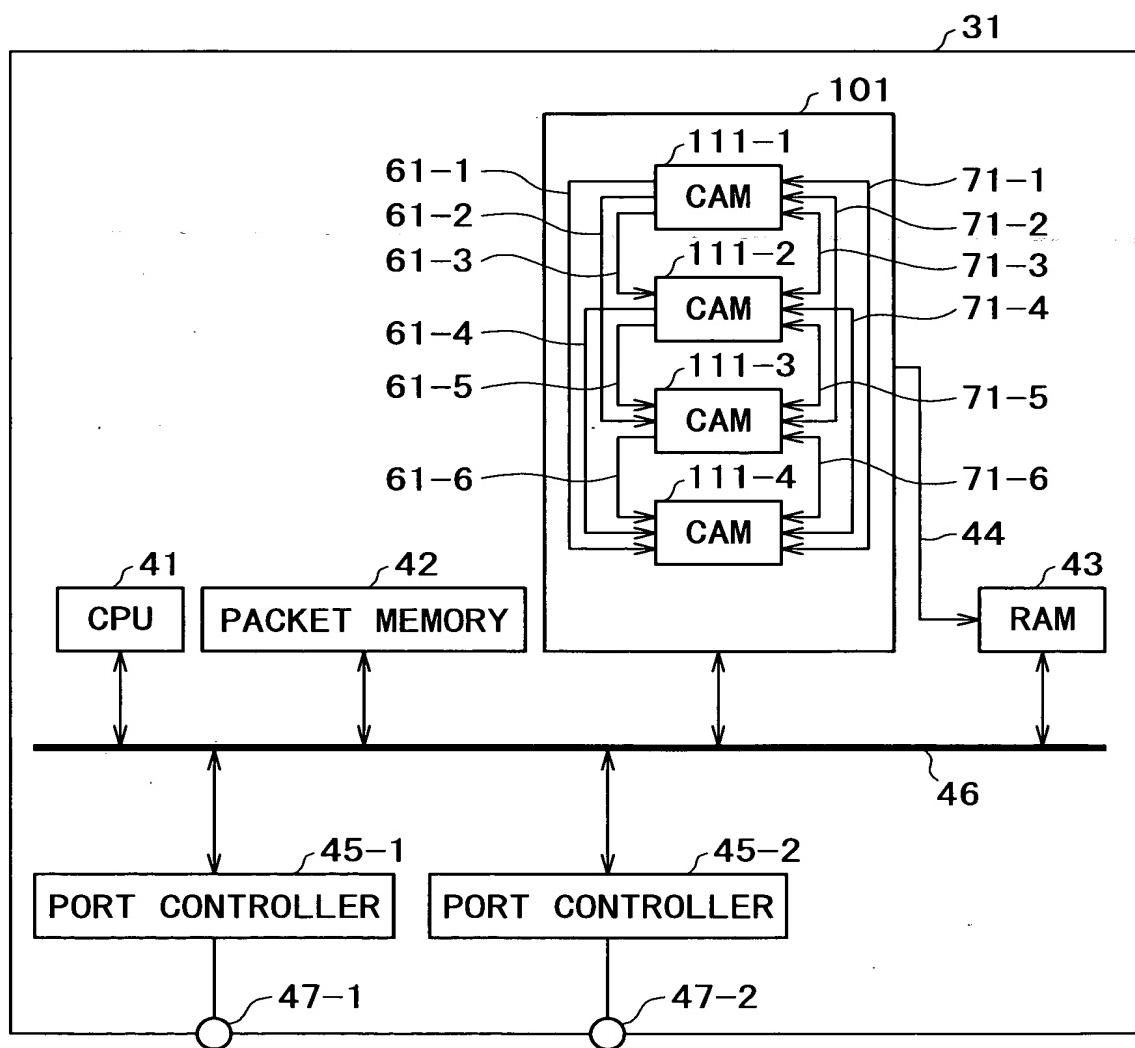


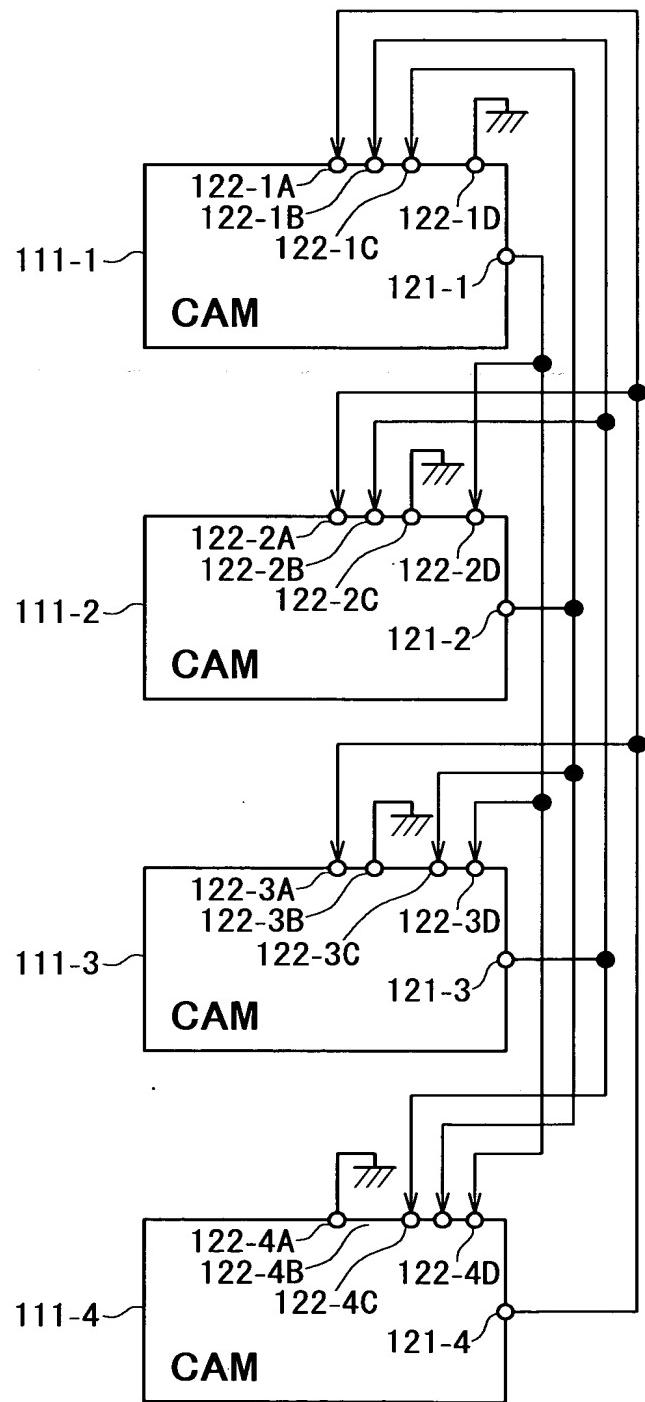
FIG. 10



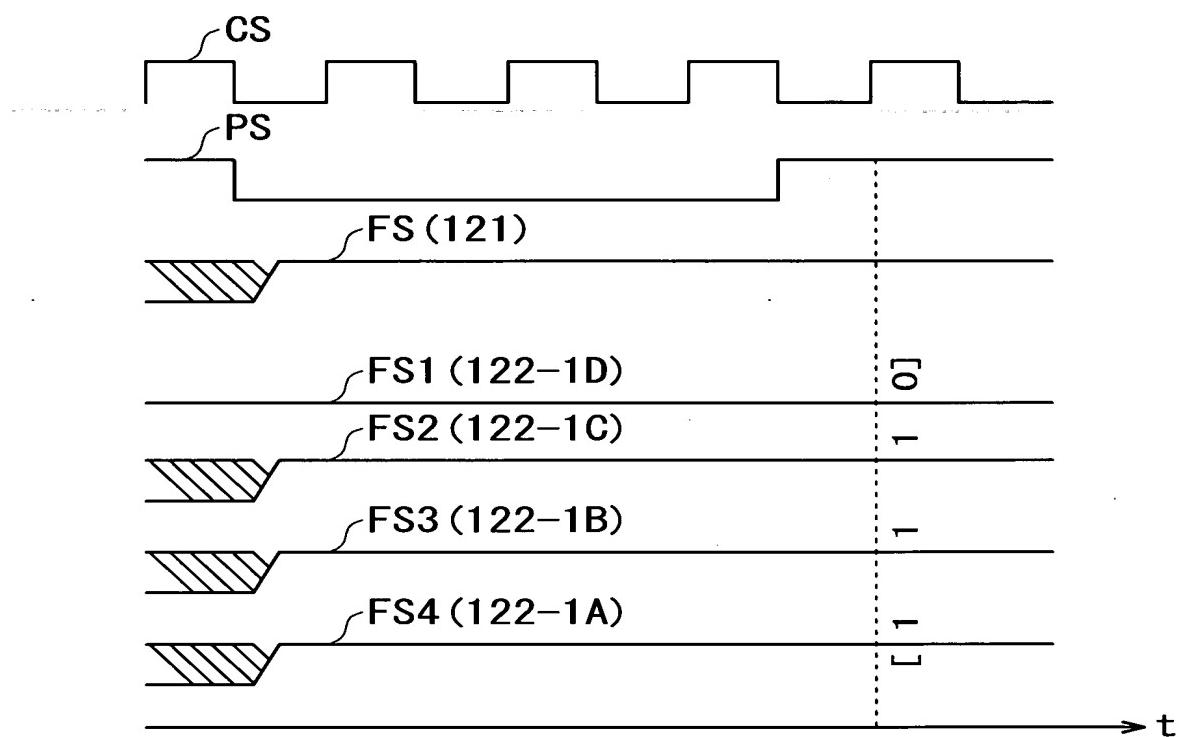
F I G. 1 1



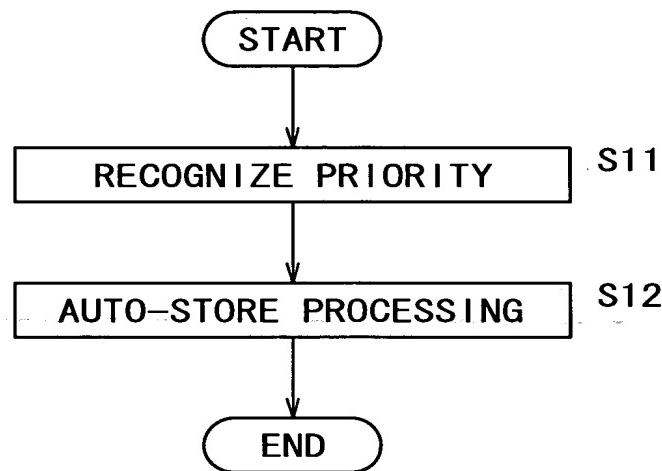
## F I G. 1 2



F I G. 1 3



F I G. 1 4



F I G. 1 5

INPUT SIGNAL [ABCD]	PROCESSING
[1110]	INTERNAL HIT
[1101]	INPUT SIGNAL[D] !=0&&, INTERNAL HIT
[1011]	INPUT SIGNAL[C] !=0&&, INPUT SIGNAL[D] !=0&& INTERNAL HIT
[0111]	INPUT SIGNAL[B] !=0&&, INPUT SIGNAL[C] !=0&& INPUT SIGNAL[D] !=0&&, INTERNAL HIT

FIG. 16

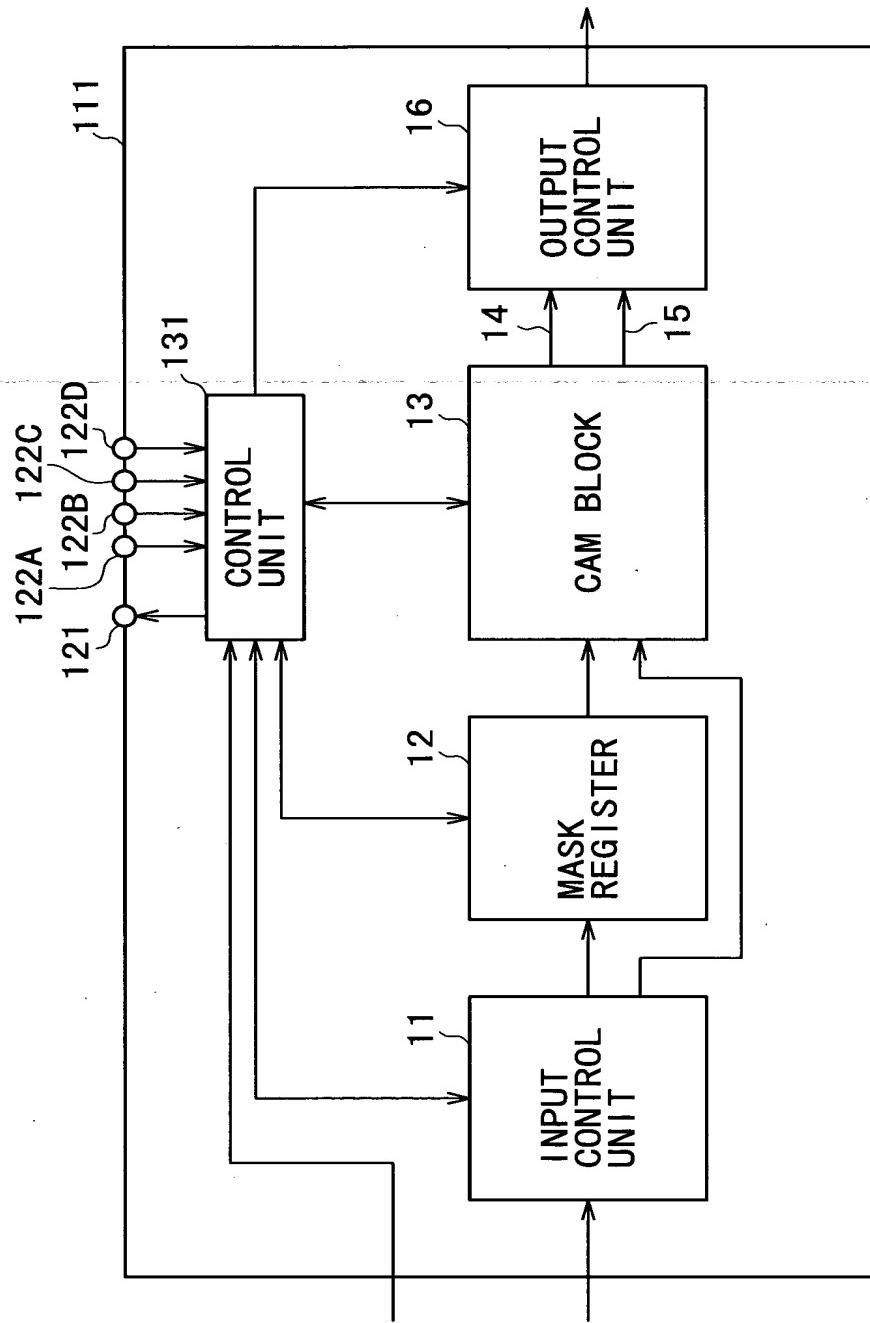
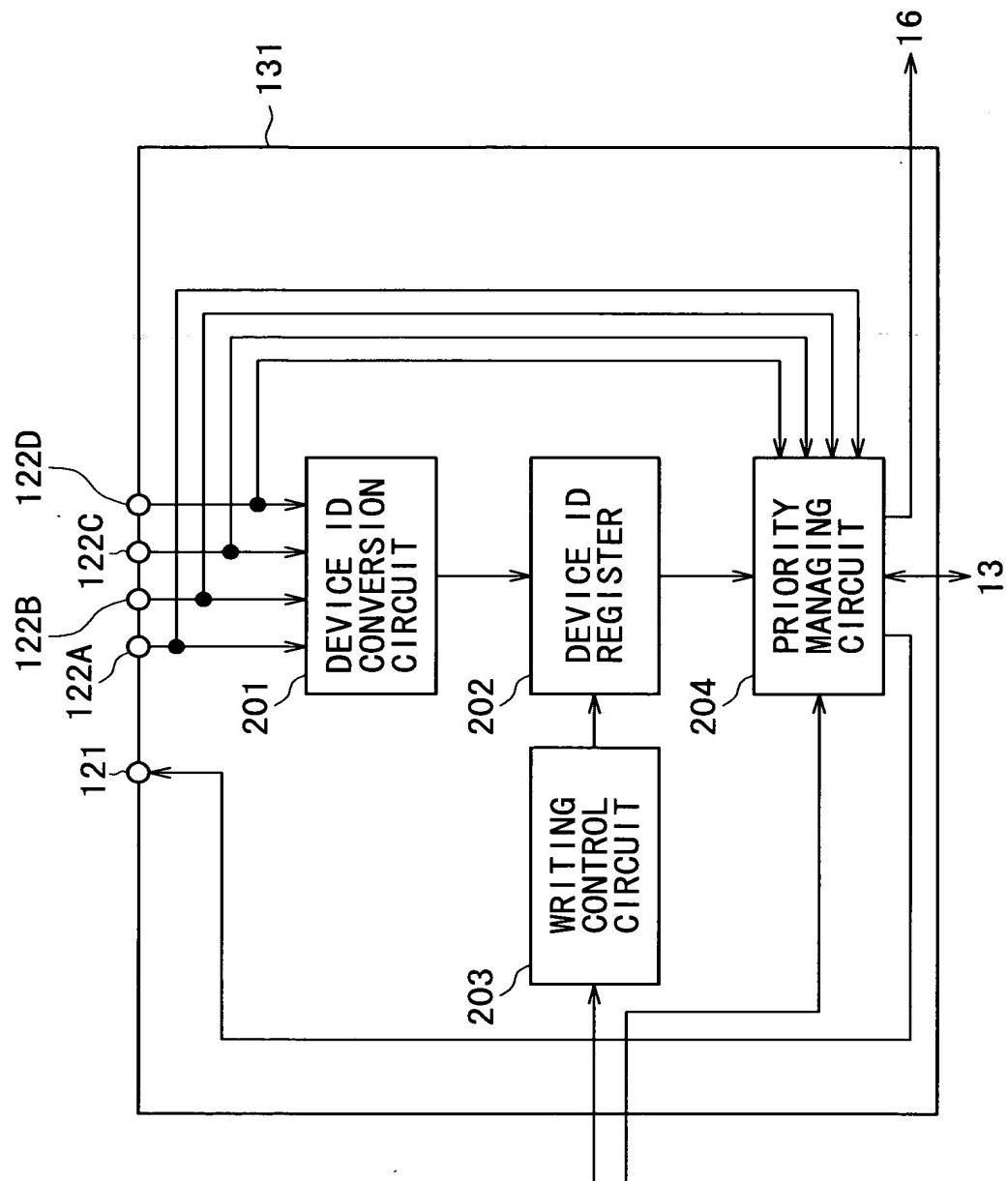


FIG. 17



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F I G. 1 8

INPUT SIGNAL [ABCD]	DEVICE ID
[1110]	0
[1101]	1
[1011]	2
[0111]	3